REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the subject application. The Final Office Action of July 14, 2003 and the Advisory Action of November 14, 2003 have been received and their contents carefully reviewed.

In the Final Office Action dated July 14, 2003, the Examiner rejected claims 1-26 under 35 U.S.C. §102(e) as being anticipated by Moon (U.S. Pat. No. 5,793,346). This rejection is traversed and reconsideration of the claims is respectfully requested in view of the following remarks.

> In the Final Office Action of July 14, 2003, the Examiner rejects claims 1, 9, 11, and 19, citing Moon as teaching "a screen clearing circuit 40 connected at an input to the gate driving circuit 10 wherein the controller 30 controls gate driving circuit 10, which supplies gate on/off voltages sequentially through the gate lines to the thin film transistors 70 (column 4, lines 12-23, figure 6 at 10, 30). Furthermore, the gate on/off generator 50 generates the Voff and Von voltages which are sent to the gate lines by the gate driving circuit 10 (column 4, lines 23-25, figure 6 at 10, 50) wherein the screen clearing circuit 40 is connected to the Voff output of gate on/off generator 50 (column 4, lines 25-26). When the external power is disconnected, the screen clearing circuit 40 operates to discharge the storage capacitors 80 connected to the gate lines (column 4, lines 27-29)." (Office Action at 3.)

Assuming *arguendo* that Moon actually teaches the elements as asserted above by the Examiner, Applicants respectfully submit Moon fails to anticipate at least the inventions defined in claims 1, 9, 11, and 19. It is respectfully submitted that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference. Moreover, the identical invention must be shown in as complete detail as is contained in each claim. Stated another way, the claimed elements must be arranged as required by each claim. See M.P.E.P. § 2131.

Claim 1 is allowable over Moon in that claim 1 recites a combination of elements including, for example, "...thin film transistors defining liquid crystal cells... connected to... gate lines and... data lines...; level shifting means for receiving a power supply and a ground voltage to apply a first voltage level for turning off the thin film transistors to the gate lines upon power-on and to apply a higher voltage level than the ground voltage to the gate lines upon power-off." Moon fails to teach, either expressly or inherently, at least these features of the claimed invention. Accordingly, Applicants respectfully submit that claims 2-8, which depend from claim 1, are also allowable over Moon.

Claim 9 is allowable over Moon in that claim 9 recites a combination of elements including, for example, "A residual image eliminating method for a liquid crystal display device including thin film transistors connected between gate lines and data lines... the method comprising... receiving a power supply voltage and a ground voltage to apply a first voltage level for turning off the thin film transistors to the gate lines upon power-on; and applying a higher level voltage than the ground voltage to the gate lines upon power off." Moon fails to teach, either expressly or inherently, at least these features of the claimed invention. Accordingly, Applicants respectfully submit that claim 10, which depends from claim 9, is also allowable over Moon.

Claim 11 is allowable over Moon in that claim 11 recites a combination of elements including, for example, "...liquid crystal cells, each liquid crystal cell having a thin film transistor, ...a gate voltage generator having a transistor connected between a first voltage source and a second voltage source to generate a gate-off voltage at an output; and a voltage enhancing device having a capacitor coupled to the output and the second voltage source, wherein when the first voltage source is turned on, the capacitor is charged and when the first

voltage source is turned off, the capacitor boosts the gate off voltage at the output to be higher than a threshold voltage of the thin film transistor." Moon fails to teach, either expressly or inherently, at least these features of the claimed invention. Accordingly, Applicants respectfully submit that claims 12-18, which depend from claim 11, are also allowable over Moon.

Claim 19 is allowable over Moon in that claim 19 recites a combination of elements including, for example, "...liquid crystal cells, each liquid crystal cells having a thin film transistor; ...a gate-off voltage generator having a transistor connected between a first voltage source and a second voltage source to generate a gate-off voltage at an output; and a voltage enhancing device having a capacitor coupled to the output and the second voltage source, wherein when the first voltage source is turned on, the capacitor is charged and when the first voltage source is turned off, the capacitor boosts the gate off voltage at the output to be higher than a threshold voltage of the thin film transistor." Moon fails to teach, either expressly or inherently, at least these features of the claimed invention. Accordingly, Applicants respectfully submit that claims 20-26, which depend from claim 19, are also allowable over Moon.

In the Advisory Action of November 14, 2003, the Examiner appears to support the rejection held in the Final Office Action by stating that Moon

> "...[teaches the] concept of applying a gate-off voltages upon applying an external power VDD by teaching how the Node N1 shows a ground level 0V when external 5V power is being supplied... while it shows (-5V), when the external power is shut off (see Moon at column 3, lines 39-42, figures 4 & 5). Furthermore, Moon teaches how this node N1 functions to turn off the transistors M1 which are connected to the gate lines. Specifically, Moon teaches that when the voltage level of node N1 is 0V, the gate-source voltage Vgs becomes greater

> than the threshold voltage Vth of the PMOS transistor M1 (column 3, lines 45-47). This causes this transistor M1 to be turned off (column 3, lines 47-48). Clearly Moon teaches a mechanism of supplying a gate-off voltage upon applying an external VDD."

Preliminarily, Applicants respectively submit that, while Moon teaches at column 3, lines 39-42, wherein "Node N1 shows a ground level 0V when external 5V power VDD is being supplied... [and] shows (-5V)... when the external power is shut off," Moon is completely silent as to any application of gate-off voltages related to PMOS transistor M1, as asserted by the Examiner. While the PMOS transistor M1 may be connected to the gate lines, Applicants respectfully submit Moon is silent as to the equivalence of the PMOS transistor M1 to the TFTs within the LCD panel. Further, Applicants respectfully submit that one of ordinary skill in the art would readily recognize that applying gate-off voltages to thin film transistors included within liquid crystal cells is not equivalent to causing a PMOS transistor M1 within a screen clearing circuit 40 to turn off upon shutting off an external power source of a liquid crystal display device.

Secondly, and assuming *arguendo* that Moon teaches wherein the PMOS transistor M1 within the screen clearing circuit 40 is turned off when "...the voltage level of node N1 is 0V [because] the gate-source voltage Vgs becomes greater than the threshold voltage Vth of the PMOS transistor M1," as asserted by the Examiner, Applicants respectfully submit that such a phenomenon does not constitute the application of a gate-off voltage "upon applying an external VDD," as asserted by the Examiner.

Regardless of whether or not the PMOS transistor M1 of the screen clearing circuit 40 of Moon is turned off in response to an applied gate-off voltage upon applying an external VDD, Applicants respectfully submit Moon fails to teach a device or a method wherein a

voltage for turning off thin film transistors within liquid crystal cells of liquid crystal display devices is applied to thin film transistors within the liquid crystal cells of the liquid crystal display device upon power-on (as, for example, claimed in claims 1, 9, 11, and 19). Similarly, Applicants respectfully submit that Moon fails to teach at least the aforementioned elements that are actually claimed in the present inventions (e.g., a device that applies a voltage higher than ground voltage to gate lines upon power-off, as claimed in claim 1; a method of applying a voltage higher than ground voltage to gate lines upon power-off, as claimed in claim 9; a device having a capacitor, wherein upon turning off a voltage source, the capacitor boosts the gate off voltage to be higher than a threshold voltage of a thin film transistor within a liquid crystal cell of a liquid crystal display device, as claimed in claims 11 and 19; etc.).

Applicants believe the application is in condition for allowance and early, favorable action is respectfully solicited. Should the Examiner deem that a telephone conference would further the prosecution of this application, the Examiner is invited to call the undersigned attorney at (202) 496-7500.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. § 1.136. Please credit any overpayment to deposit Account No. 50-0911.

Respectfully submitted,

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Date: 4-13-03

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